Attorney Docket No. 108298630US

#13

Express Mail Label EV139295839US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:	Setho Sing Fee *et al.*	EXAMINER:	Tu Tu Ho
APPLICATION NO.:	09/944,246	ART UNIT:	2818
FILED:	30 August 2001	CONF. NO:	1798

FOR: **PACKAGED MICROELECTRONIC DEVICES AND METHODS OF FORMING SAME**

Declaration of Prior Invention Under 37 C.F.R. § 1.131

Assistant Commissioner for Patents
Washington, D.C. 20231

1. This Declaration establishes invention in Singapore prior to 18 July 2001.

2. This Declaration is being made by Setho Sing Fee, Lim Thiam Chye, and Eric Tan Swee Seng, i.e., the inventors named in this application.

3. Before 18 July 2001, we conceived the invention currently presented in claims 1, 2, 6-9, 11, 12, 15, 17, 18, 22, 23, 32, and 33 of the above-identified patent application; a listing of these claims is attached as Exhibit A. Our conception of the invention is corroborated by the following documents:

   a) Micron Electronics, Inc. Invention Disclosure Form 0532 (the "0532 Disclosure") attached as Exhibit B. The dates next to each of our signatures on each page in Exhibit B have been blacked out, but each of those dates is prior to 18 July 2001.

   b) A drawing entitled "104 LEAD LPGA (14.0 X 20.1 X 0.76) mm PCKAGE OUTLINE" and a drawing entitled "104 LEAD LPGA (14.0 X 20.1 X 0.76) mm LEADFRAME" (collectively, the "LPGA Drawings") attached as Exhibit C. Each of the LPGA Drawings bears a date which has been blacked out, but which is prior to 18 July 2001.

Exhibit D. The dates in the Estimated Project Timeframe have been blacked out, but at least the first two phases include dates which are prior to 18 July 2001.

4. As shown in the 0532 disclosure, as of a date prior to 18 July 2002 we conceived of a stacked microelectronic device assembly that includes several subassemblies, each of which includes a die having an exposed back surface, lead fingers having exposed front and back contacts, and an encapsulant. The LPGA Drawing and the Assembly Baseline illustrate that, prior to 18 July 2001, we also conceived processes for manufacturing such an assembly. These processes include the use of a peel-off tape and cutting the leadframe to singulate the packaged dies.

5. After conceiving this invention, we proceeded diligently by preparing and filing the 0532 Disclosure with my employer, working through an initial invention review procedure, and participating in the preparation and filing of Singaporean Application No. 200105297-6 on 29 August 2001 and the filing of the above-identified application on 30 August 2001.

6. Each of us declares that all statements made herein of his or her own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, (18 U.S.C. §1001) and that such willful false statements may jeopardize the validity of this application or any patent issued thereon.

Setho Sing Fee

Date 10/31/02
Residence: Republic of Singapore
Citizenship : Republic of Singapore
P.O. Address : Block 91, Bedok North Street 4, #11-1523
Singapore 460091

Lim Thiam Chye

Date 10/31/2002

Residence: Republic of Singapore
Citizenship : Republic of Singapore
P.O. Address : Block 224, Simei Street 4, #11-98
Singapore 520224

Eric Tan Swee Seng

Date 10/31/2002

Residence: Republic of Singapore
Citizenship : Republic of Singapore
P.O. Address : Block 106, Pasir Ris Street 12, #03-109
Singapore 510106

Exhibit A

1. A method of assembling a microelectronic device assembly, comprising:
releasably attaching a support to a lead frame, the lead frame having a thickness and having an opening passing through the thickness, the support having an exposed surface spanning the opening;
releasably attaching a back surface of a microelectronic device to the exposed surface of the support;
electrically coupling the microelectronic device to the lead frame;
delivering an encapsulant to a cavity defined by the support, the microelectronic device, and a peripheral dam carried by the lead frame, the encapsulant bonding the microelectronic device to the lead frame; and
removing the support, leaving the back surface of the microelectronic device exposed.

2. The method of claim 1 further comprising cutting the lead frame within a periphery defined by the peripheral dam to separate a plurality of electrically isolated lead fingers.

6. The method of claim 1 wherein the active surface of the die is coupled to the lead frame by a plurality of bond wires.

7. The method of claim 6 wherein an upper surface of the encapsulant is aligned with the upper surface of the lead frame and the bond wires are encapsulated in the encapsulant.

8. The method of claim 1 wherein removing the support exposes a lower surface of each of a plurality of lead fingers.

9. The method of claim 1 wherein removing the support exposes a lower surface of each of a plurality of lead fingers, the exposed lower surfaces being peripherally aligned.

11. The method of claim 1 wherein the lead frame includes a plurality of lead fingers extending inwardly from the peripheral dam, the encapsulant being permitted to flow between the support and at least some of the lead fingers.

12. A method of assembling a microelectronic device assembly including a microelectronic die and a plurality of electrically independent lead fingers, comprising:

releasably attaching a first support to a back surface of a first lead frame and to a back surface of a first microelectronic die, the first lead frame including a front surface spaced from the back surface and an opening extending from the front surface to the back surface, the opening having an inner periphery defined by a first outer member and a plurality of first lead fingers extending inwardly from the first outer member, the first die being positioned in the opening with a periphery of the first die spaced inwardly of at least part of the inner periphery of the opening to define a first peripheral gap;

electrically coupling the first die to the first lead fingers with a plurality of first bonding wires;

filling the opening above the first support with a first encapsulant, the first encapsulant entering the first peripheral gap and attaching the first lead frame to the first die; and

removing the first support, leaving the back surface of the first die exposed and leaving the back surface of the first lead frame exposed.

15. The method of claim 12 wherein the first support comprises an adhesive tape, the first lead frame and the first die being releasably adhered to the adhesive tape and the adhesive tape forming a seal against the back surface of the first lead frame and the back surface of the first die to retain the first encapsulant.

17. The method of claim 12 further comprising:

releasably attaching a second support to a back surface of a second lead frame and to a back surface of a second microelectronic die, the second lead frame

including a front surface spaced from the back surface and an opening extending from the front surface to the back surface, the opening having an inner periphery defined by a second outer member and a plurality of second lead fingers extending inwardly from the second outer member, the second die being positioned in the opening with a periphery of the second die spaced inwardly of at least part of an inner periphery of the opening to define a second peripheral gap;

electrically coupling the second die to the second lead fingers with a plurality of second bonding wires;

filling the opening above the second support with a second encapsulant, the second encapsulant entering the second peripheral gap and attaching the second lead frame to the second die;

removing the second support, leaving the back surface of the second die exposed and leaving the back surface of the second lead frame exposed; and

electrically coupling one of the first lead fingers to one of the second lead fingers.

18. The method of claim 17 wherein a plurality of the first lead fingers are electrically coupled to a plurality of the second lead fingers.

22. The method of claim 17 wherein electrically coupling the first and second lead fingers spaces the second die from the first encapsulant to define an intercomponent gap between the second die and the first encapsulant.

23. The method of claim 17 wherein the first lead finger is electrically coupled to the second lead finger by electrically coupling a front surface of the first lead finger to a back surface of the second lead finger.

32. A stacked microelectronic device assembly, comprising:

a first subassembly having a first thickness and comprising a plurality of electrically independent first lead fingers, a first die, and a first encapsulant

bonding the first die to the first lead fingers, each of the first lead fingers having a thickness equal to the first thickness and defining an exposed front contact and an exposed back contact, the first die having an exposed back surface and being electrically coupled to the plurality of first lead fingers by a plurality of first bonding wires;

a second subassembly having a second thickness and comprising a plurality of electrically independent second lead fingers, a second die, and a second encapsulant bonding the second die to the second lead fingers, each of the second lead fingers having a thickness equal to the second thickness and defining an exposed front contact and an exposed back contact, the second die having an exposed back surface and being electrically coupled to the plurality of second lead fingers by a plurality of second bonding wires;

a plurality of electrical connectors, each of which electrically couples the exposed front contact of one of the first lead fingers to the exposed back contact of one of the second lead fingers.

33. The stacked microelectronic device assembly of claim 32 wherein an intercomponent gap is defined between the first and second subassemblies.

EXHIBIT B

Received [redacted]

INVENTION DISCLOSURE

RECEIVED [redacted]

[redacted] 0532

1.A. **INVENTOR(S):** 1) Setho Sing Fee
Micron Semiconductor Asia Private Limited
sethosf@micron.com

Home Address: Block 91, Bedok North Street 4, #11-1523
Singapore 460091
Republic of Singapore

Citizenship: Republic of Singapore

[redacted]

1.B. **INVENTOR(S):** 2) Lim Thiam Chye
Micron Semiconductor Asia Private Limited
sltc@micron.com

Home Address: Block 224, Simei Street 4, #11-98
Singapore 520224
Republic of Singapore

Citizenship: Republic of Singapore

[redacted]

1.C. **INVENTOR(S):** 3) Eric Tan Swee Seng
Micron Semiconductor Asia Private Limited
erictanss@micron.com

Home Address: Block 106, Pasir Ris Street 12, #03-109
Singapore 510106
Republic of Singapore

Citizenship: Republic of Singapore

[redacted]

2. **DESCRIPTION:**

- **Title:**

Thin Leadless Package (TLP).

- **Brief Description: As Illustrated in Fig. 1, 2 & 3.**

1. Fig 1 & 2 shows the TLP configuration.

2. It is a low profile package where the package height is actually the leadframe thickness prior to plating.

3. The package can be stacked. Fig 3 shows an example of a stack package configuration. The number of stack packages is not limited to three packages as shown.

- **Propose :**

1. To provide a low profile and small footprint package.

2. To facilitate component level stacking.

3. CONCEPTION & DOCUMENTATION OF INVENTION:

- **Date when Invention was first conceived:**
  Feb 9, 2001
- **To whom was the idea first described:**
  Lim Thiam Chye
- **Date of the first tangible record:**
  Feb 9, 2001
- **Type & location:**
  Inventor's Notebook. (No.101972)

4. INFORMATION RELATED TO INVENTION:

- **Related invention disclosure:**
  None
- **Closest technology:**
  None
- **Advantages of this invention over previous technology:**

1) To provide a low profile and small footprint package.

2) To facilitate component level stacking.

5. IMPORTANT DATES:

- **If the invention has been disclosed outside the company, please specify to whom it has been disclosed, when, and in what format:**
  N/A
- **If any articles describing your invention have been published, please specify the author(s), title of article, publication and date:**
  N/A
- **If any engineering samples have been given out, please specify to whom and on what date they were given:**
  None

6. **DISPOSITION OF THE INVENTION:**

- **When will (or did) Micron begin use of the invention experimentally:**
  Year 2001
- **When will (or did) Micron begin production of this invention:**
  To be determined

7. **MISCELLANEOUS INFORMATION:**

- **ARPA project:**
  NO
- **Was the invention developed during a joint development agreement or other contract with an outside company:**
  NO
- **List developmental work outside of the company, including Government proposal or contract:**
  None

8. **INVENTORS:**

1) Setho Sing Fee
Principal Package Development Engineer
Employee# 793303

2) Lim Thiam Chye
Packaging Development Section Manager
Employee# 766631

3) Eric Tan Swee Seng
Packaging Development Engineer

Employee# 793369

9. **WITNESS:**

If there is only one (1) inventor. a witness should sign and date this disclosure. A witness in this case is a non-inventor who understands the nature of the invention.

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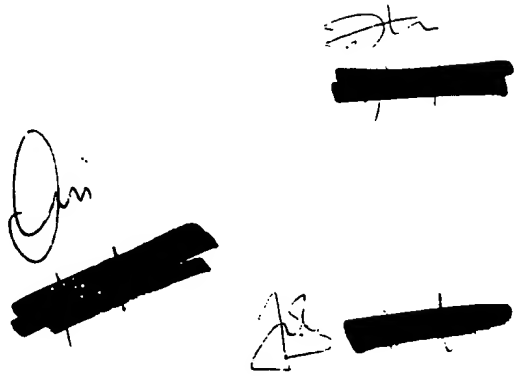
(Signature of Witness) (Date)



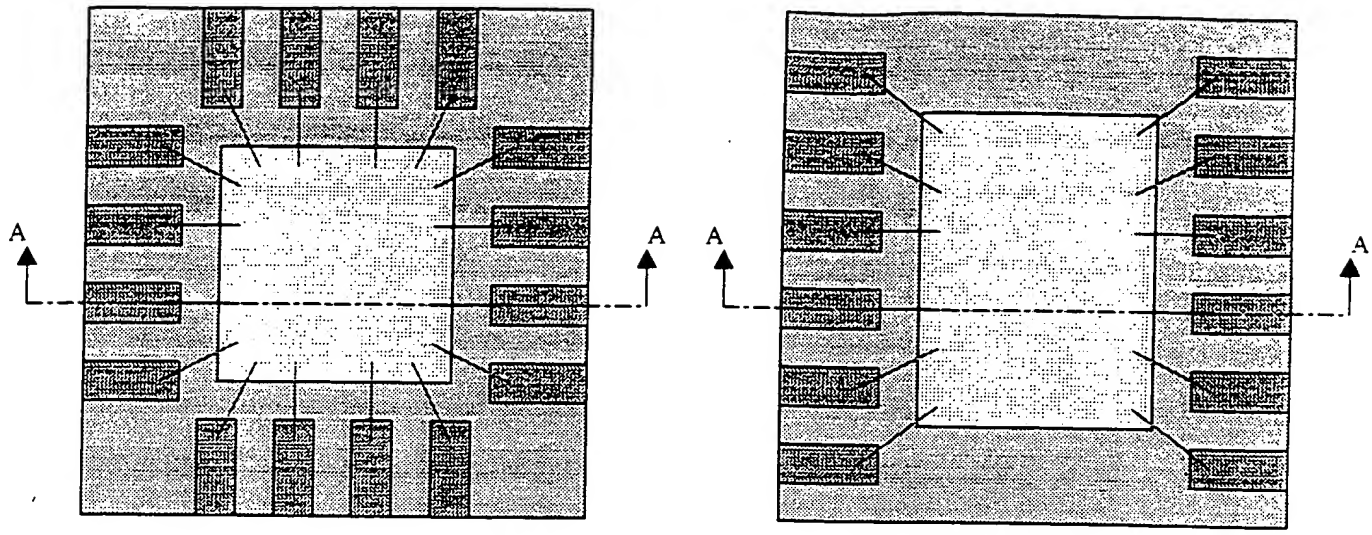


Fig 1 : TLP Constructional Layout (Quad & Dual lead version)

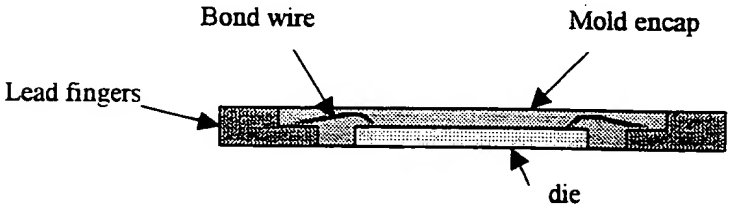


Fig 2 : Cross-Sectional A-A View of Package

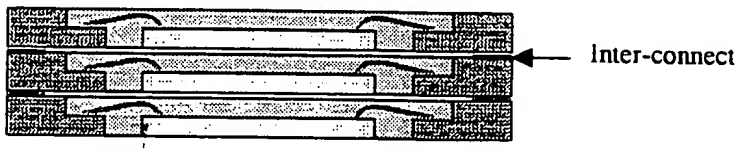
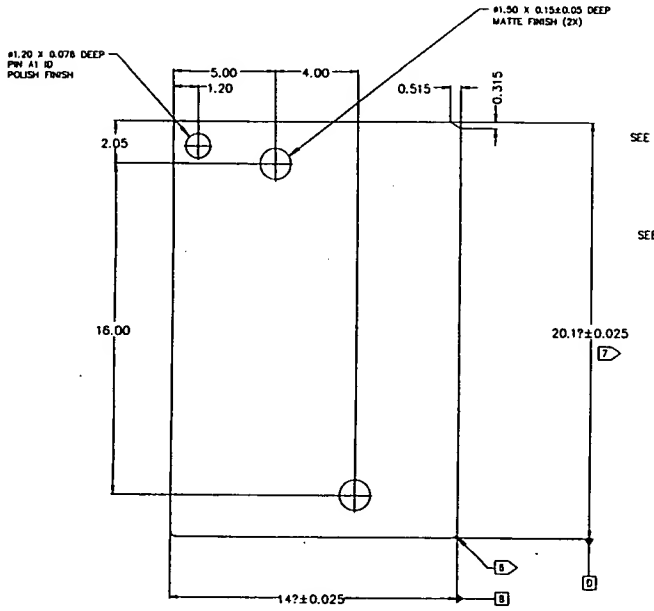
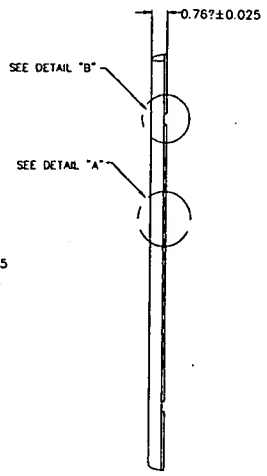
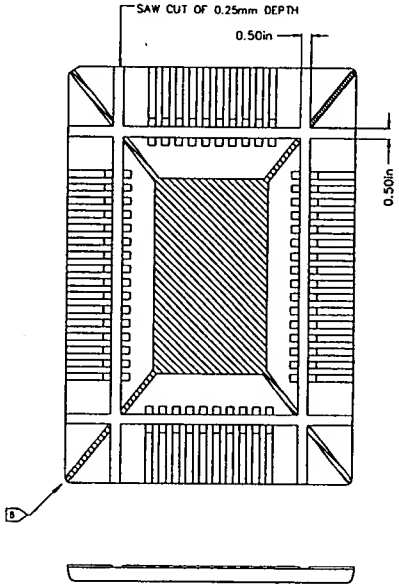


Fig 3 : TLP Stack Package Configuration

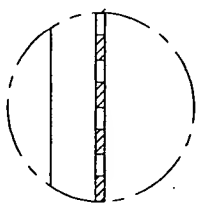
EXHIBIT C



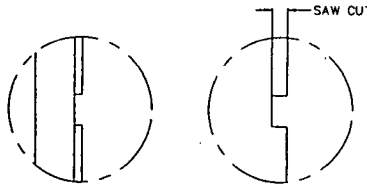




	NOTES
1	DIMENSIONS ARE IN MILLIMETERS. DIMENSIONS IN ( ) ARE FOR REFERENCE ONLY.
2	LEADFRAME MATERIAL: OLIN 7025 COPPER, 0.127±0.007 THICK.
3	MATTE FINISH ALL SIDES, 118-72 MICROMETERS Ra
4	MOLDED BODY DIMENSIONS APPLY AFTER POST MOLD STABILIZATION BAKE, 14 HRS
5	LEAD COPLANARITY: 0.05 MAXIMUM
6	ALL MOLDED BODY CORNER RADII TO BE 0.254 MAXIMUM UNLESS OTHERWISE SPECIFIED.
7	MAXIMUM MISMATCH OF TOP TO BOTTOM OF MOLDED BODY TO BE 0.050 IN ANY DIRECTION. MAXIMUM TOP AND BOTTOM MOLDED BODY OFFSET FROM DIE PAD CENTER TO BE 0.050 IN ANY DIRECTION. DATUM DIMENSIONS [D] AND [E] INCLUDE MOLD MISMATCH. FOR TRUE POSITION CALL-OUT SEE UNIT MOLDED STRIP ON SHEET 2.
8	BASIC DIMENSION REFERS TO TIP TO TIP LOCATION
9	BODY DIMENSIONS EXCLUDE EDGE FLASH ON ALL FOUR SIDES. FLASH TO BE CONTROLLED BY LEADFRAME, MOLD SPECIFICATION AND TRIM/FORM SPECIFICATION.
10	[E] REFERS TO TOP OF LEAD AS IT EXITS THE PACKAGE BODY.
11	LEAD FINISH: TIN/LEAD PLATING 80/20, 400-1100 MICROINCHES THICK PER SIDE
12	ALL PACKAGES TO BE IDENTIFIED WITH NUMERIC CHARACTER ON THE BOTTOM SIDE OF PIN ONE INDICATOR. REFERENCE MICRON DRAWING 026-00-0075
13	MOLDED BODY MATERIAL: EPOXY NOVOLAC
14	TOTAL SURFACE AREA TO BE PLATED: 5457.72 SQ. MM
15	LEAD LENGTH CUT SHALL BE BURR UP.
16	DAMBAR CUT TO REMAIN CONSISTENT WITHIN 0.013 ON ALL LEADS
17	MAXIMUM MICRO GAP BETWEEN LEAD AND MOLDED PLASTIC BODY SHALL NOT EXCEED 7 MICRONS.
18	THIS CONTROL FEATURE APPLIES AFTER DE-DAMBAR AND BEFORE FINAL FORM.



DETAIL A
SCALE: 35 :1



DETAIL B
SCALE: 35 :1

PRELIMINARY

[redacted]

ELECTRONIC FILE

NO.	DESCRIPTION	BY	APP.	DATE

REVISIONS

NO.	DESCRIPTION	BY	APP.	DATE

REFERENCE BLOCK	
CAD-REF	XXXXXXX-X.MI

DESIGNED: XX	XXXX
DRAWN: XX	XXXX
CHECKED:	

TOLERANCES
UNLESS OTHERWISE SPECIFIED
.XX ± 0.05
.XXX ± 0.05
.XXXX ± 0.025
ANGLE ± 5°

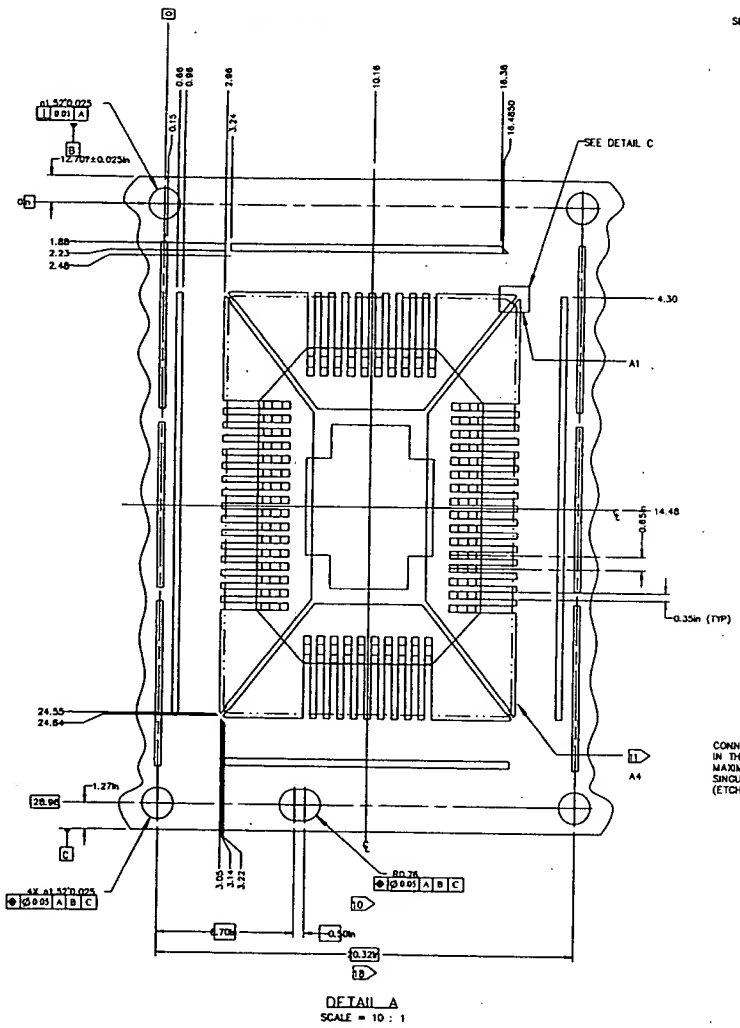
104 LEAD LPGA
(14.0 X 20.1 X 0.76)mm
PCKAGE OUTLINE

NOTE

YES	SILVER PLATING MIN: 0.0015–MAX: 0.0120	42 ALLOY (0.127 THK)	XXX-XXXXX
TAPE OPTION	FINISH	MATERIAL	SAP NUMBER

Micron SEMICONDUCTOR ASIA PTE LTD
990 Bendemeer Road,
Singapore 339942
Tel: (65) 299 3000 Fax: (65) 299 3184

DRAWING NO. XXX-XX-XXXXX
REVISIONS —
MICRON PART NO. —
SCALE: 10 : 1
SHEET 1 OF 2



DETAIL A
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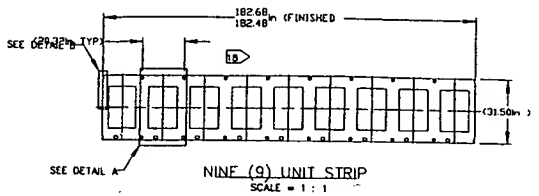
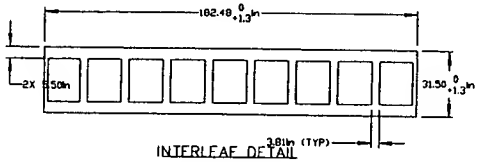
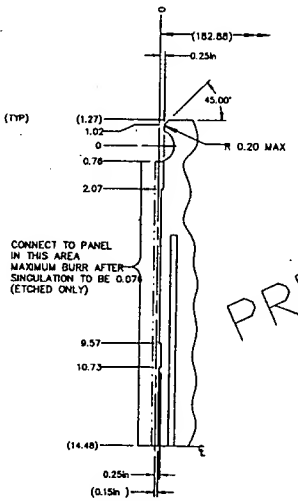


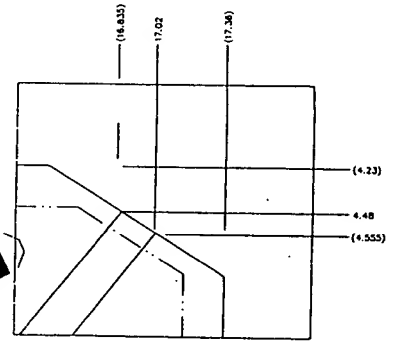
NINE (9) UNIT STRIP
SCALE = 1 : 1



INTERLEAF DETAIL
SCALE = 1 : 1



DETAIL B
SCALE = 10 : 1



DETAIL C
SCALE = 100 : 1

PRELIMINARY

NOTES	
1	DIMENSIONS IN MM. DIMENSIONS IN ( ) ARE FOR REFERENCE ONLY.
2	LEADFRAME MATL: COPPER ALLOY 7025, HALF HARD, 0.250t±0.007 THK.
3	THIN SILVER PLATING: 130t±40 MICROINCHES PER INDICATED DIMENSIONS.
4	MARK MICRON PART NUMBER IN INDICATED AREA. USE ENTIRE PART NUMBER EXCEPT THE FIRST FOUR DIGITS.
5	INT AND LEADTIP RADII TO BE 0.127 MAX, EXT RADII 0.254 MAX (STAMPED). LEADTIP RADII 0.127 MAX, INT RADII 0.152 MAX, EXT RADII 0.254 MAX (ETCHED).
6	
7	SHEET 5 IS NOT REQUIRED TO MANUFACTURE THE LEADFRAME.
8	STAMPED PART SHALL BE BURR UP.
9	NO SPANKING OR TOOL MARKS TO BE WITHIN 2.286 OF THE LEADTIPS. COINING ALLOWED ONLY ON TOP SIDE OF LEADTIPS PER INDICATED DIMENSIONS.
10	THIS AREA TO BE USED FOR STAMPING LOGO OR OTHER NUMBERS IF NEEDED.
11	DATUM PLANE "A" TO BE ESTABLISHED AT FOUR (4) DATUM TARGET POINTS. WHILE FRAME IS CLAMPED WITH MICRON DESIGNED FIXTURE.
12	
13	WINDOW MUST BE LARGE ENOUGH TO AVOID ALL "OUT-OF-PLANE" FEATURES. INTERLEAF MUST NOT CONTACT SILVER PLATING AND ENDS MUST BE CLOSED.
14	DOWNSET DEPTH TOLERANCE APPLIES FROM BOTTOM OF BEND TO BOTTOM OF BEND.
15	SPECIFIC RADIUS DIMENSIONS: "a" = R 0.076.
16	
17	
18	TOLERANCE SHALL NOT BE ACCUMULATIVE OVER LENGTH OF THE STRIP.

NO.	DESCRIPTION	BY	APP.	DATE

REVISIONS

NO.	DESCRIPTION	BY	APP.	DATE

REFERENCE BLOCK	
CAD-REF	406100xx-11

DESIGNED:
DRAWN:
CHECKED:

TOLERANCES
UNLESS OTHERWISE SPECIFIED
.X ± 0.05
.XX ± 0.05
.XXX ± 0.025
ANGLE ± 5'

ELECTRONIC FILE

YES	SILVER PLATING MIN: 0.0015–MAX: 0.0120	42 ALLOY (0.25 THK)	330-000xx
TAPE OPTION	FINISH	MATERIAL	SAP NUMBER

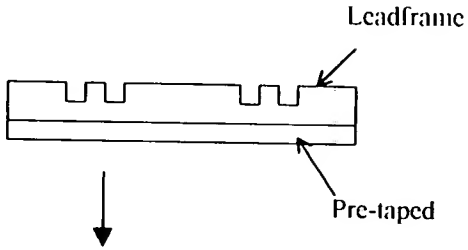
104 LEAD LPGA
(14.0 X 20.1 X 0.76)mm
LEADFRAME

Micron
SEMICONDUCTOR ASIA PTE LTD
990 Bendemeer Road,
Singapore 339942
Tel: (65) 299 3000 Fax: (65) 299 3100

DRAWING NO.	REVISIONS
025-06-1000x	C
MICRON PART NO.	–
SCALE: AS NOTED	SHEET 1 OF 2

Assembly Baseline

Leadframe Design



Team Members

Designer - [redacted] (R & D Engineering)
- [redacted] (Pkg Dev Engineering)

Material - [redacted] (Pkg Dev Engineering)

Challenge
- Leadframe, die pad, support bar and frame layout configuration.
- Plating type(Ag, Pd), thickness and layer
- Stamped or etched leadframe
- Material of leadframe (Electrical, thermal and mechanical properties
- Selection of pre-tape material

Die Bank

Backgrind

Wafer Mount

} Process - [redacted]
} Equipment - [redacted]

Exhibit D

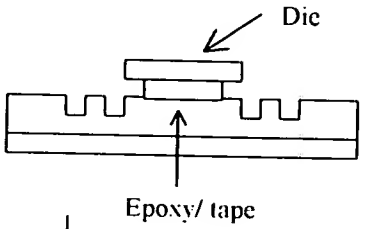
Wafer Saw

↓

UV Cure

↓

Die Attach

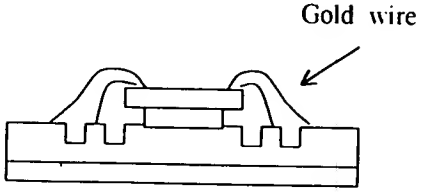


↓

Epoxy Cure

↓

Wire Bond



↓

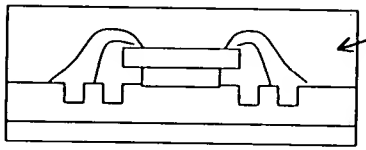
Process - [redacted] (Pkg Tech Dev Engineering)
Equipment - [redacted] (Equipment Engineer)
Challenge - Epoxy / tape selection
- cure profile optimisation

Process - [redacted] (Pkg Tech Dev Engineering)
Equipment - [redacted] (Equipment Engineer)
Challenge - Plating thickness, layer and type selection
- Elasticity of the laminated films absorbs too much of the bond energy, resulting in significant strength decrease.

Pre-Mold Inspection

↓

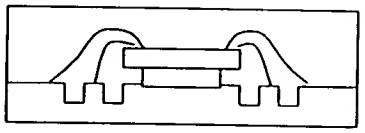
Encapsulation



Process - [redacted] (Pkg Tech Dev Engineering)
Equipment - [redacted] (Equipment Engineer)
Challenge - Mold compund selection for adhesion strength
- warpage, mold bleed/flash
- FAM (Film assisted molding)

↓

De-tape



Challenge - Residue free peel off properties from leadframe and mold compound
- No standard equipment, requires manual operation

↓

Strip Laser

↓

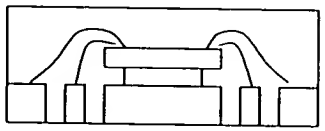
Post Encapsulation Cure

↓

Solder Plating

↓

Singulation



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VM Inspection

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O/S Test

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PCB Mounting

Process - [redacted](Process Engineering)
Challenge - Deflash and strip plating

Process - [redacted](Pkg Tech Dev Engineering)
Equipment - [redacted](Equipment Engineering)
Challenge - Selection of saw blade to cut leadframe (Alloy or copper)
- reduce smearing of leads, top, bottom, side chipping
- blade life and feedrate

Process – [redacted]

Module group - Bridging
- Solder joint integrity
- Asymmetric device standoff caused by tension of the solder joint after reflow. (Paste optimization and solder pad design)

Estimated Project Timeframe

1. Internal leadframe design review : [redacted]
2. Supplier leadframe design review : [redacted]
3. Final leadframe design review : [redacted]
4. Tooling up:
   a. Leadframe : [redacted]
   b. Die Attach : [redacted]
   c. Wire Bond : [redacted]
   d. Encapsulation : [redacted]
   e. Singulation : [redacted]
5. Assembly checkout (Daisy chain) : [redacted]
6. Open-short test : [redacted]
7. Reliability look ahead : [redacted]
8. Others